EGC220
Class Notes
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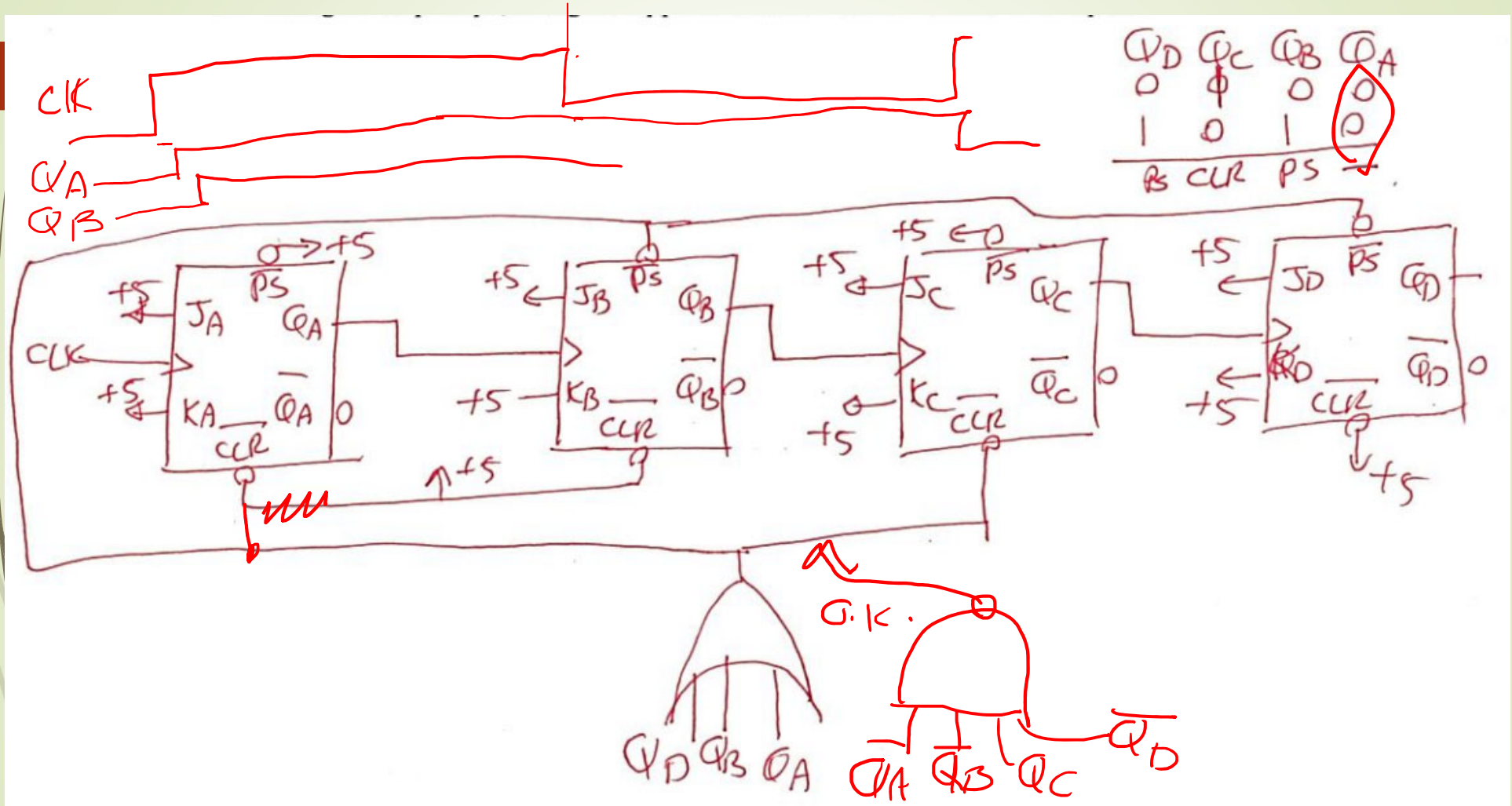
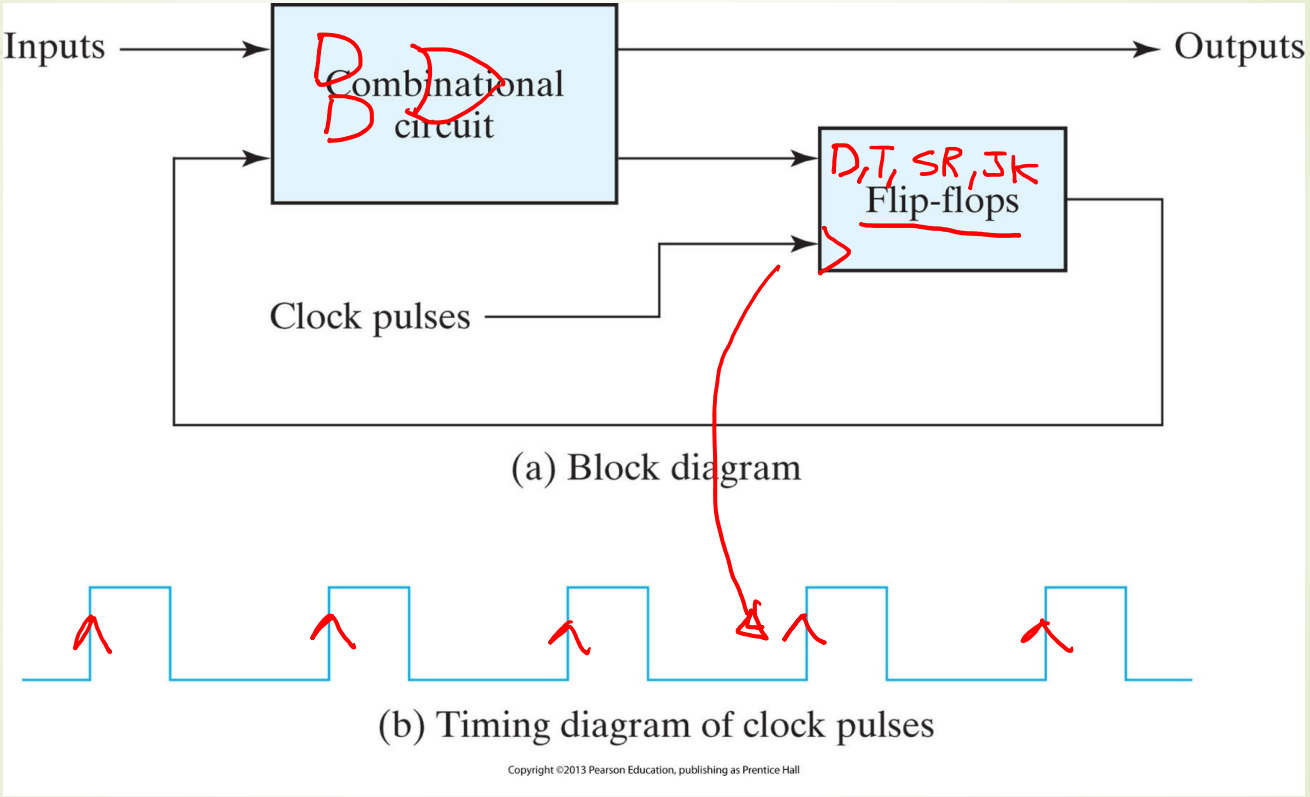
Test 2 will cover the following topics

- Design of combinational circuits
  - Circuit conversion to all NAND or NOR gates
- Design and use of
  - Multiplexers
  - Demultiplexers
  - Decoders
  - Encoders
- Design of combinational circuits using PLD's
- Latch and flip flops characteristics and timing.
- Design of ripple counters
- Analysis of sequential circuits


CLK
Q_A
Q_B
Q_D Q_C Q_B Q_A
0 0 0 0
1 0 1 0
$\overline{PS}$ $\overline{CLR}$ PS
+5
J_A
K_A
Q_A
J_B
K_B
Q_B
J_C
K_C
Q_C
J_D
K_D
Q_D
$\overline{PS}$
$\overline{CLR}$
0
G.K.
Q_D Q_B Q_A
Q_A Q_B Q_C Q_D

Synchronous Circuit



How do we determine its functionality?

Flip Flops Vs. Latches

- Flip flops are Edge Triggered
- ~~Latches are level triggered~~

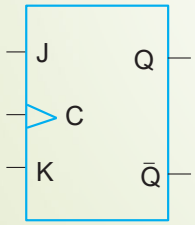
only use F/F for design & analysis

(a) *JK* Flip-Flop

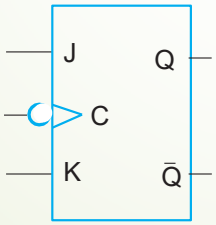
J	K	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}(t)$	Complement

(b) *SR* Flip-Flop

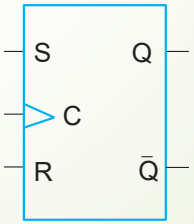
S	R	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined



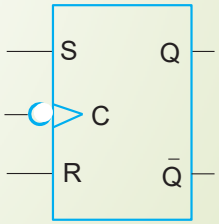
Triggered JK



Triggered JK



Triggered JK



Triggered JK

Flip Flops Vs. Latches

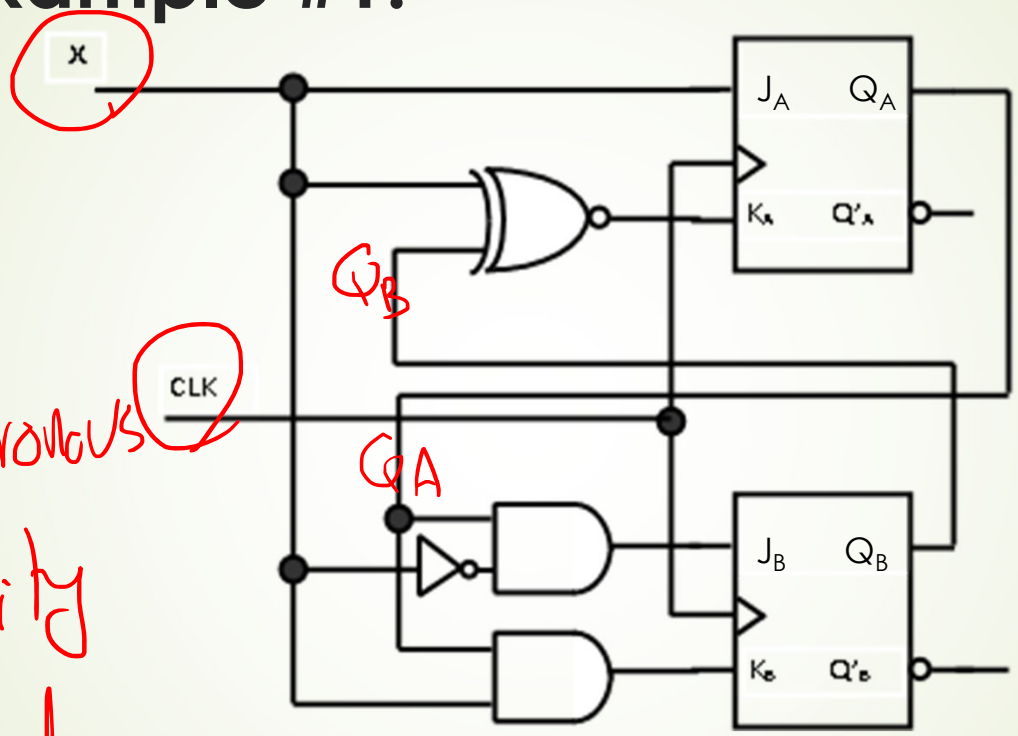
- Flip flops are Edge Triggered
- Latches are level triggered

(c) *D* Flip-Flop			(d) *T* Flip-Flop		
D	***Q* (*t* +1)**	**Operation**	**T**	***Q* (*t* +1)**	**Operation**
0	0	Reset	0	$Q(t)$	No change
1	1	Set	1	$\overline{Q}(t)$	Complement

Analysis of Sequential Circuits

- **Analysis Procedure:**
  - **Obtain flip-flop input equations**
  - **Write down characteristic table of each type of flip-flop in use**
  - **Develop state table**
  - **Obtain state diagram**

Example #1:



system input

Q_B

synchronous

Q_A

Functionality does not depend on ↑ or ↓ CLK.

Step 1: Flip-flop input equations and output equation

$J_A = X$

$K_A = \overline{Q_B \oplus X}$

$J_B = Q_A X'$

$K_B = Q_A X$

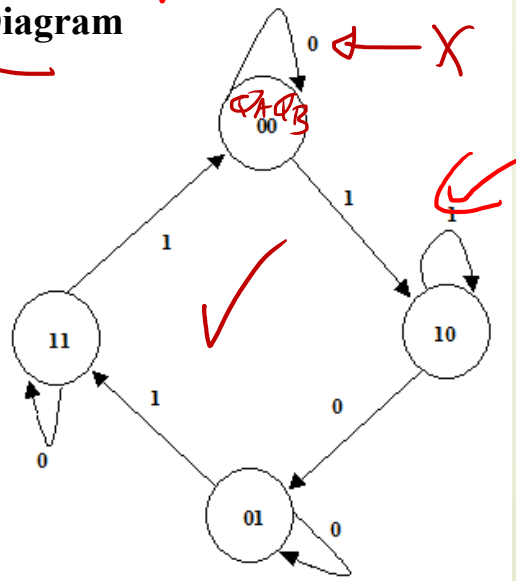
Step 2: Characteristic Table

J K	Q(t+1)
0 0	Q(t)
0 1	0
1 0	1
1 1	Q'(t)

Step 3: State Table

PS Q_A Q_B	X	J_A	K_A	J_B	K_B	NS Q_A Q_B
0	0	0	1	0	0	0 0
0	1	1	0	0	0	1 0
0	0	0	0	0	0	0 1
0	1	1	1	0	0	1 1
1	0	0	1	1	0	0 1
1	1	1	0	0	1	1 0
1	0	0	0	1	0	1 1
1	1	1	1	0	1	0 0

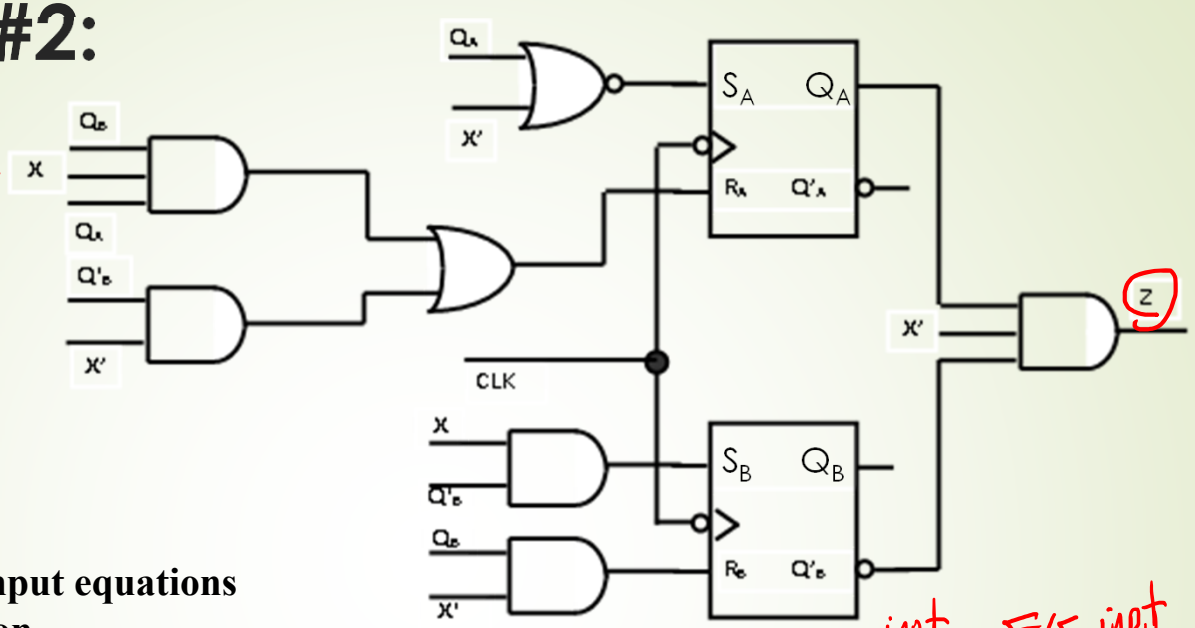
Step 4: State Diagram



Example #2:

X: system input

Z: system output



Step 1: Flip-flop input equations and output equation

$S_A = (Q_A + X')' = Q'_A X$

$R_A = Q_A Q_B X + Q'_B X'$

$S_B = Q'_B X$

$R_B = Q_B X'$

$Z = Q_A Q'_B X'$

Step 2: Characteristic Table

S R	Q(t+1)
0 0	Q(t)
0 1	0
1 0	1
1 1	--

PS input	F/F input	NS	output
$Q_A Q_B X$	$S_A R_A S_B R_B$	$Q_A Q_B$	Z
0 0 0	using F/F input equations	using F/F input & chara. table	using equ.
⋮			
1 1 1			

Problem 1

Analyze the following sequential circuits leading to a state diagram.

$J_A = K_A = Q_B Q_C X + \bar{Q}_B \bar{Q}_C \bar{X}$ ✓

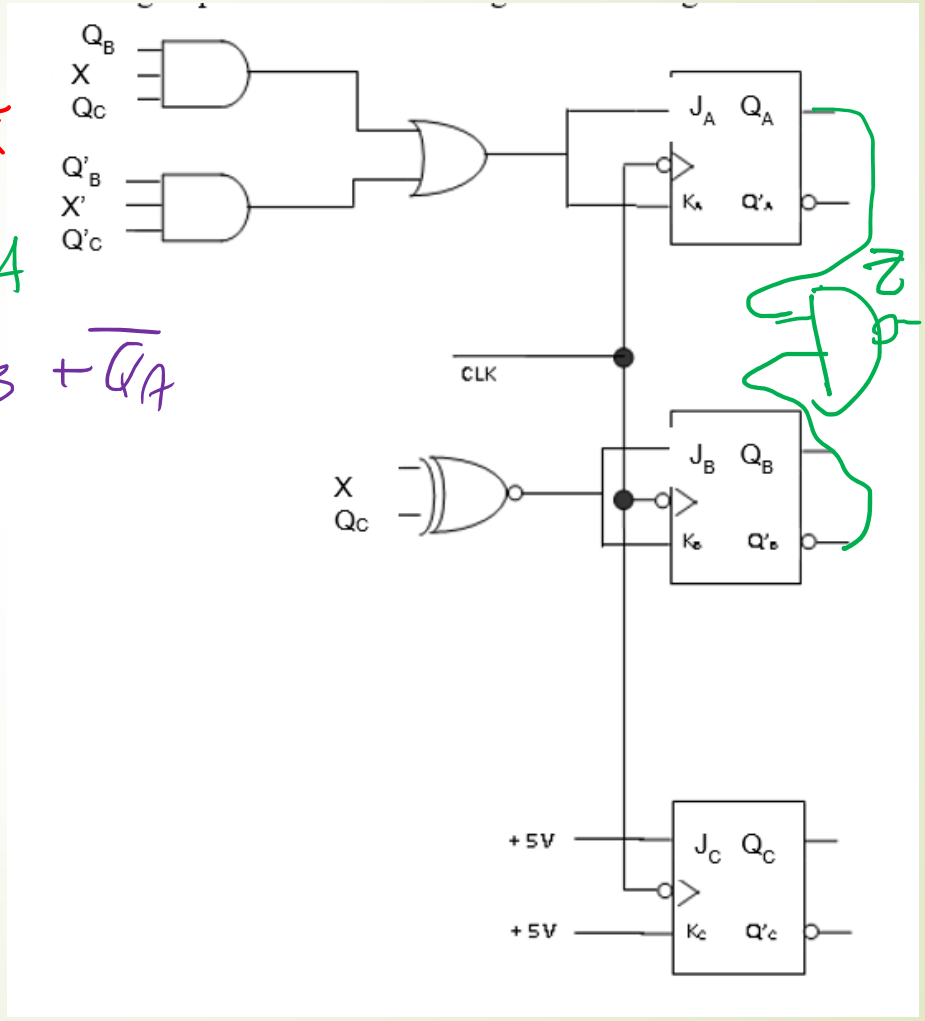
$J_B = K_B = X \odot Q_C = \overline{Q_C \oplus X}$

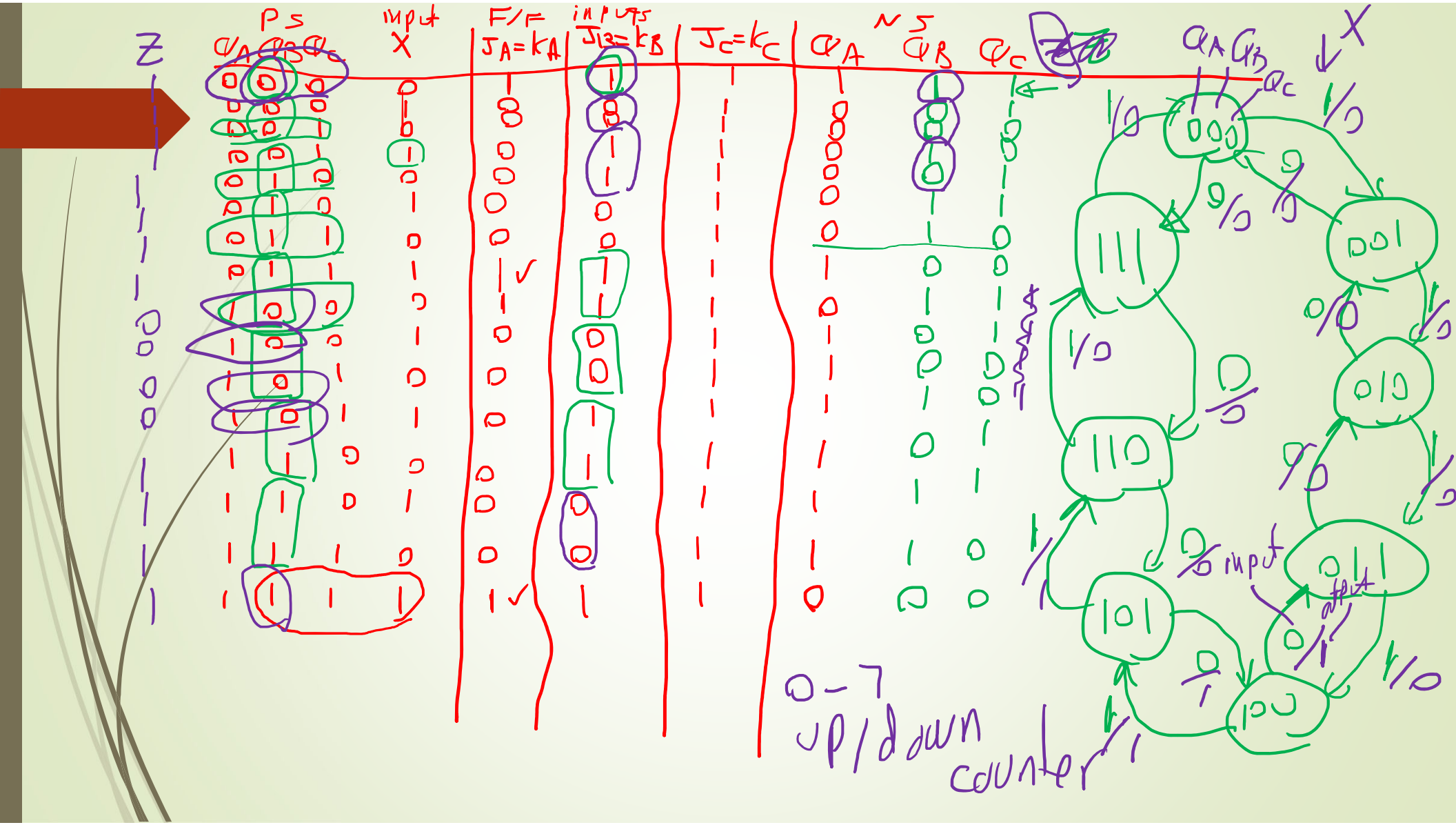
$J_C = K_C = 1$

$Z = \bar{Q}_B Q_A = \bar{Q}_B Q_A$

$Q_B + \bar{Q}_A$

J	K	Q (t +1)
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\bar{Q}(t)$




Z
PS
$Q_A Q_B Q_C$
input
X
F/F inputs
$J_A = k_A$
$J_B = k_B$
$J_C = k_C$
NS
Q_A
Q_B
Q_C
$Q_A Q_B$
Q_C
X
1/0
0/1
0-7
up/down
counter
input

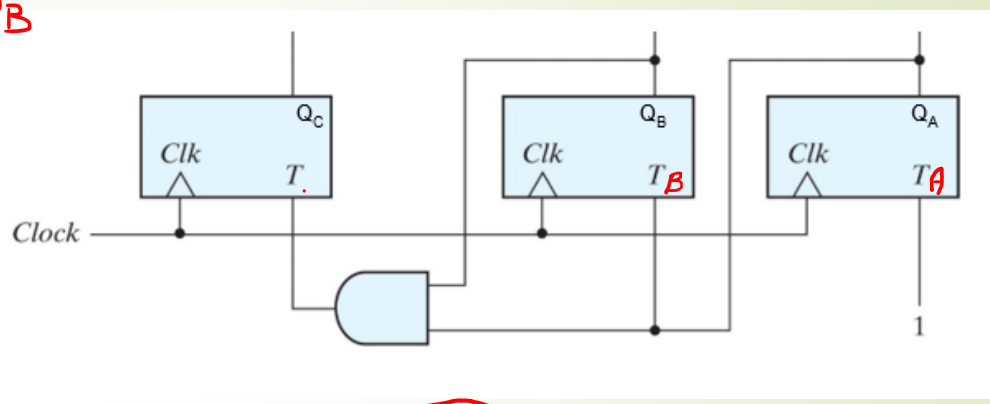
Problem 2

Analyze the following sequential circuits leading to a state diagram.

1. $T_A = 1$; $T_B = Q_A$; $T_C = Q_A Q_B$

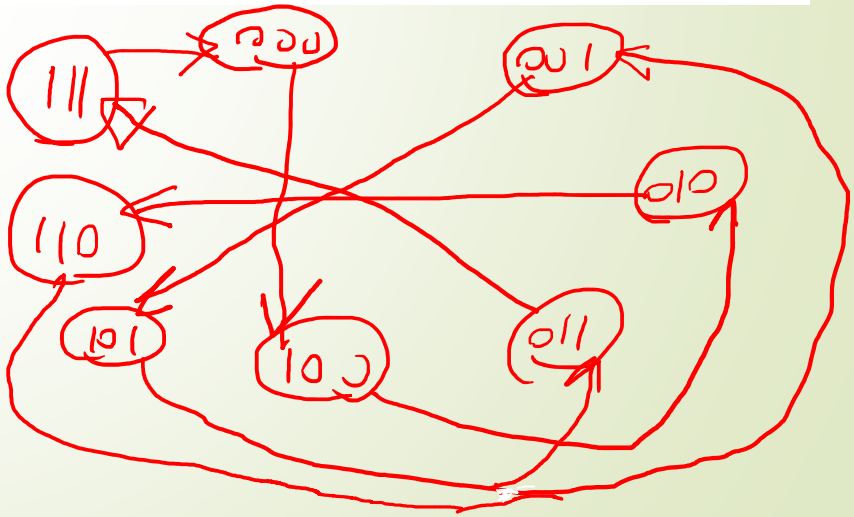
2.

T	Q(t+1)
0	Q(t)
1	Q'(t)



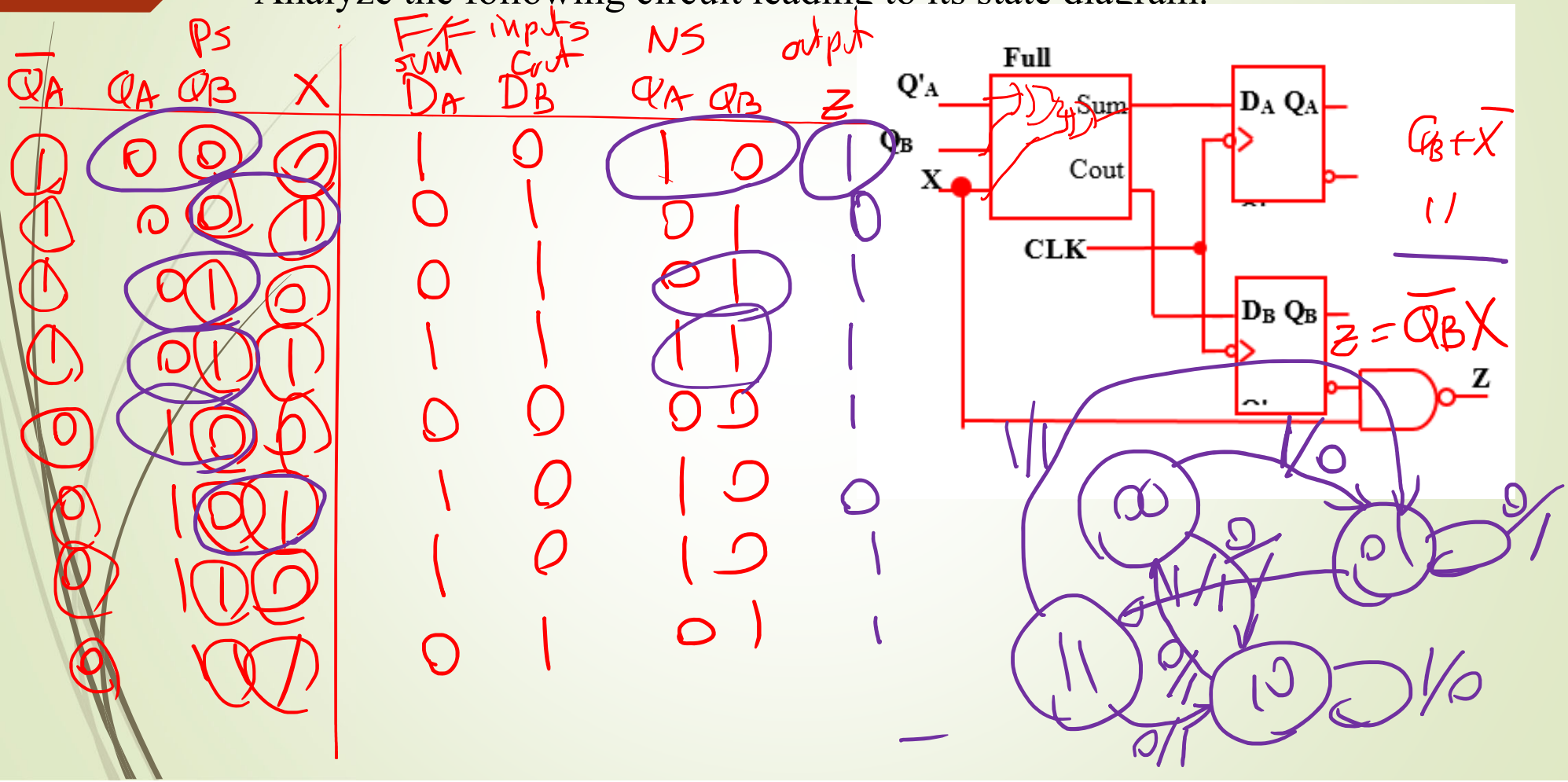
3.

PS			NS			T_A	T_B	T_C
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C			
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



Problem 3

Analyze the following circuit leading to its state diagram.



Data flow

assign → equation.

behav. ← CLK

describe ckt

@ (x, ^, x)

case